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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/743,121
Filing Date: December 22, 2003
Appellant(s): ALBEROLA ET AL.

Patrick J. Buckley, Reg. No. 40,928
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 8/21/2007 appealing from the Office action mailed 3/8/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

The examiner notes that the claim objections and the drawing objections for claims 1, 8, 16, and 21 are withdrawn due to the appellant's amendment filed on 7/9/2007.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Kotani et al. (U.S. 6,789,140), Pechanek et al. (U.S. 6,848,041), Kessler et al. (U.S. 6,738,836), Ramsdale et al. (U.S. 5,265,263), Funderbunk et al. (U.S. 5,291, 525), and Dent (U.S. 6,229,796) are relied upon as evidence.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

New Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 5-9, 11, and 14-17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kotani et al. (U.S. 6,789,140), in view of Pechanek et al. (U.S. 6,848,041).

3. As per claim 1:

Kotani disclosed a method, comprising:

Retrieving a first instruction from a memory unit via an n-bit input path (Kotani: Figure 9 element 20, column 10 lines 25-48)(The DMA unit receives drawing data and commands from main memory to transfer to the processing unit. It's inherent that the instructions received by DMA unit are received via a n-bit bus.);

Pre-decoding the first instruction at a direct memory access unit (Kotani: Figure 9 element 234, column 11 lines 51-64)(The DMA pre-decodes instructions in order to look

for interrupts before transferring the instructions and data to the processing unit.); and

Providing the pre-decoded first instruction from the direct memory access unit to a processing element via a q-bit output path (Kotani: Figure 9 element 232, column 10 lines 34-48 and column 11 lines 51-64)(The DMA pre-decodes instructions in order to look for interrupts before transferring the instructions and data to the processing unit, either directly or through the local memory element 40 in figure 9. It's inherent that the instructions received by DMA unit are sent out via a q-bit bus).

Decoding the pre-decoded first instruction at the processing element (Kotani: Figure 9 element 232, column 10 lines 34-48)(It's inherent that the processing element fully decodes the command instruction in order to know how the instructions are supposed to operate in the drawing unit.); and

Executing the decoded instruction via a processor pipeline (Kotani: Figure 9 element 232, column 10 lines 34-48)(The drawing unit inherently executes the instructions it receives.).

Determining, based on said executing, that a second instruction subsequent to the first instruction will not be executed (Kotani: Figure 11 element 239, column 11 lines 20-28)(The drawing end instruction tells that there are no further instructions to execute in the current path. It's obvious to one of ordinary skill in the art that the DMA controller will continually fetch instructions from a current memory area until told to do otherwise. Therefore, the DMA will only be told to do so otherwise at the very earliest when the drawing end instruction is predecoded within the DMA. Since Kotani doesn't disclose the predecoder being used for detecting the drawing end instruction, it's obvious to one

of ordinary skill in the art that the drawing end instruction may not be detected until it's fully decoded in the processor. Thus, it would have been obvious to one of ordinary skill in the art that at least one more instruction would have been fetched from memory during the predecoding process, which leaves at least one instruction within the DMA that won't be executed because the drawing has finished processing.); and

Arranging for a pre-decoded second instruction to not be provided from the direct memory access unit to the processing element (Kotani: Figure 11 element 239, column 11 lines 20-28)(The drawing end instruction tells that there are no further instructions to execute in the current path. It's obvious to one of ordinary skill in the art that the DMA controller will continually fetch instructions from a current memory area until told to do otherwise. Therefore, the DMA will only be told to do so otherwise at the very earliest when the drawing end instruction is predecoded within the DMA. Since Kotani doesn't disclose the predecoder being used for detecting the drawing end instruction, it's obvious to one of ordinary skill in the art that the drawing end instruction may not be detected until it's fully decoded in the processor. Thus, it would have been obvious to one of ordinary skill in the art that at least one more instruction would have been fetched from memory during the predecoding process, which leaves at least one instruction within the DMA that won't be executed because the drawing has finished processing. Also, it's obvious to one of ordinary skill in the art that this instruction would come into the DMA and be predecoded in the next cycle.).

Kotani failed to teach where the n-bit input path is less than the q-bit output path;.

However, Pechanek disclosed where the n-bit input path is less than the q-bit

output path (Pechanek: Figure 5 element 512, column 10 lines 37-43)(An example instruction, the add instruction, is predecoded by element 512, which generates control signals. When in combination with Kotani, these control signals would also be sent with the instruction to the processor, which results in a larger output path than the input path.).

Kotani is silent on the details of how predecoding works. Pechanek describes the details of predecoding an instruction that results in control signals for the processor being generated by the predecoder. One of ordinary skill in the art would have been motivated to find out how predecoding works to find the processor of Pechanek that describes in detail the generation of control signals for instructions to add this functionality. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to add the control signal generation aspect of Pechanek for the advantage of realizing how predecoding works.

4. As per claim 2:

Kotani and Pechanek disclosed the method of claim 1, wherein said providing comprises storing the pre-decoded first instruction in memory local to the processing element (Kotani: Figure 9 element 40, column 10 lines 34-48 and column 11 lines 51-64)(The DMA pre-decodes instructions in order to look for interrupts before transferring the instructions and data to the processing unit, either directly or through the local memory element 40 in figure 9.).

5. As per claim 5:

Kotani and Pechanek disclosed the method of claim 1, further comprising:

Loading instructions into the memory unit during a boot-up process (Official notice is taken that instructions are loaded into a memory unit during a boot-up process.).

6. As per claim 6:

Kotani and Pechanek disclosed the method of claim 1, wherein the processing element is a reduced instruction set computer device (Official notice is taken that the processing element could be modified to run a RISC processor architecture.).

7. As per claim 7:

Kotani and Pechanek disclosed the method of claim 6, wherein the pre-decoded instruction comprises execution control signals (Kotani: Figure 11 element 241-242, column 11 lines 29-40)(The DMA unit pre-decodes interrupts and sends control signals back to the host processor.).

8. As per claim 8:

Claim 8 essentially recites the same limitations of claim 1. Therefore, claim 8 is rejected for the same reasons as claim 1.

9. As per claim 9:

Claim 9 essentially recites the same limitations of claim 8. Therefore, claim 9 is rejected for the same reasons as claim 8.

10. As per claim 11:

The additional limitations of claim 11 essentially recite the additional limitations of claim 2. Therefore, claim 11 is rejected for the same reasons as claim 2.

11. As per claim 14:

Kotani and Pechanek disclosed the apparatus of claim 8, wherein the direct memory access unit, the memory unit, and the processing element are formed on an integrated circuit (Official notice is taken that the DMA, memory, and PE's are formed on an integrated circuit.).

12. As per claim 15:

The additional limitations of claim 15 essentially recite the additional limitations of claim 6. Therefore, claim 15 is rejected for the same reasons as claim 6.

13. As per claim 16:

Claim 16 essentially recites the same limitations of claim 1. Therefore, claim 16 is rejected for the same reasons as claim 1.

14. As per claim 17:

Claim 17 essentially recites the same limitations of claim 2. Therefore, claim 17 is rejected for the same reasons as claim 2.

15. Claim 12 is rejected under 35 U.S.C. §103(a) as being unpatentable over Kotani et al. (U.S. 6,789,140), in view of Pechanek et al. (U.S. 6,848,041), further in view of Kessler et al. (U.S. 6,738,836).

16. As per claim 12:

Kotani and Pechanek disclosed the apparatus of claim 10, including a plurality of processing elements, each processing element being associated with a direct memory access unit that includes an instruction pre-decoder (Kotani: Figure 9 elements 232 and 234, column 10 lines 34-48 and column 11 lines 51-64).

Kotani and Pechanek failed to teach a plurality of processing elements.

However, Kessler disclosed including a plurality of processing elements (Kessler: Figure 1 element 100, column 4 lines 32-50)(Figure 1 shows a plurality of processing elements that the single processing element of Kotani could be arranged in.).

The advantage of using a large number of processing elements in parallel is that they are able to solve complex computational problems in a reasonable amount of time (Kessler: Column 2 lines 6-14). One of ordinary skill in the art at the time of the invention would have been motivated to implement a parallel computing machine comprised of processing elements of Kotani for the benefits of increased performance. Thus, one of ordinary skill in the art at the time of the invention would have made the processing element of Kotani into many elements of a large parallel computing structure for the advantage of increased performance.

17. Claim 21 is rejected under 35 U.S.C. §103(a) as being unpatentable over Kotani et al. (U.S. 6,789,140), in view of Pechanek et al. (U.S. 6,848,041), further in view of Ramsdale et al. (U.S. 5,265,263).

18. As per claim 21:

Claim 21 essentially recites the same limitations of claim 1. Claim 21 additionally recites the following limitations:

Kotani and Pechanek failed to teach a multi-directional antenna.

However, Ramsdale disclosed a multi-directional antenna (Ramsdale: Figures 1a and 1b, element 1, column 2 lines 4-13).

The advantage of having a multi-directional antenna is that it allows wireless communication between devices. One of ordinary skill in the art would have been motivated to add a multi-directional antenna to allow for wireless communication between devices. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a multi-directional antenna to allow for the processor of Kotani to have the ability to communicate wirelessly.

19. Claims 22-23 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kotani et al. (U.S. 6,789,140), in view of Pechanek et al. (U.S. 6,848,041), in view of Ramsdale et al. (U.S. 5,265,263), further in view of Funderbunk et al. (U.S. 5,291,525)

20. As per claim 22:

Kotani, Pechanek, and Ramsdale disclosed the system of claim 21.

Kotani, Pechanek, and Ramsdale failed to teach wherein the apparatus is a digital base band processor.

However, Funderbunk disclosed wherein the apparatus is a digital base band processor (Funderbunk: Figure 1, column 3 lines 50-67 continued to column 4 lines 1-37).

Base band is a method of signal transmission. The advantage of using base band is that it has a simple implementation because the signals are transmitted without frequency divisions. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the processor as a digital base band processor for the advantage of a simple implementation of transmitting signals.

21. As per claim 23:

The system of claim 22, wherein the digital base band processor is formed as a system on a chip (Official notice is given that a processor can be formed as a system on a chip.).

22. Claim 24 is rejected under 35 U.S.C. §103(a) as being unpatentable over Kotani et al. (U.S. 6,789,140), in view of Pechanek et al. (U.S. 6,848,041), in view of Ramsdale et al. (U.S. 5,265,263), further in view of Dent (U.S. 6,229,796).

23. As per claim 24:

Kotani, Pechanek, and Ramsdale disclosed the system of claim 21, wherein the system is a time-divisional multiple access base station (Ramsdale: Column 2 lines 39-48)

Kotani, Pechanek, and Ramsdale failed to teach wherein the system is a code-division multiple access base station.

However, Dent disclosed wherein the system is a code-division multiple access base station (Dent: Figure 7, column 9 lines 64-67 continued to column 10 lines 1-32).

Both time and code divisional multiple access base station are a ways of allocating frequencies among a plurality of base stations. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention that code-divisional multiple access base station could have been substituted for time-divisional multiple access base station.

(10) Response to Argument

24. Regarding claims 1, 2, 5-9, 11, and 14-17 rejected under 35 U.S.C. §103(a) as being unpatentable over Kotani et al. (U.S. 6,789,140), in view of Pechanek et al. (U.S. 6,848,041):

A.) Appellant argues "In particular, nowhere does Kotani disclose or suggest that a drawing end instruction is predecoded by the DMA controller 234. Instead, Kotani describes that "advanced" instructions, such as line drawing and filling-in of drawing areas, might be predecoded. Column 11, lines 54-64. Thus, Kotani can't been viewed as teaching "providing [a] pre-decoded first instruction from the direct memory access unit to a processing element" (where that instruction will eventually result in a determination that a subsequent instruction will not be executed)."

The examiner disagrees for the following reasons. The appellant states that Kotani disclosed that advanced instructions "might" be predecoded, while Kotani explicitly states that advanced instructions are predecoded by the direct memory access (DMA) controller (Kotani: Column 11 lines 57-61). Thus, at the very least, some of the instructions within the system are predecoded by the system of Kotani. The examiner stated in the rejection that "the first instruction" is "the drawing end instruction" of Kotani. Thus, Kotani must disclose "the drawing end instruction" is predecoded to correctly read upon the claimed limitations. Since the DMA predecodes some instructions of the processor, it's inherent that the DMA must predecode all instructions that are passed through it.

This is the case since the predecoder of the DMA is unaware of which instructions are being passed through it at any time. The only possible way that the DMA unit can tell which instructions are which is to decode the operational field of all of the instructions passing through. Thus, the DMA must predecode all instructions in order to figure out which instructions are advanced instructions. This results in the drawing end instruction being predecoded and Kotani correctly reading upon the claimed limitation.

B.) Appellants respectfully suggest that adding the details of predecoding within Pechanek onto Kotani for the advantage of realizing how predecoding works falls far short of a motivation to modify Kotani in specific ways that would result in the particular invention as recited in claim 1. Appellant also note that the general idea of "pre-decoding" could be done in any number of ways that would not require more bits in the DMA controller output path [of] Kotani as compared as compared to the input path.

The examiner disagrees there is no motivation to combine for the following reasons. Kotani disclosed generally that predecoding occurs for advanced instructions, but failed to teach the specifics of predecoding. This alone would have motivated one of ordinary skill in the art to find out how predecoding works. While the appellant disclosed that predecoding can occur in many different ways, one of ordinary skill in the art would have still been motivated to find one particular well-known type of predecoding to find Pechanek and add its functionality to Kotani.

In addition, there are many advantages of using the particular predecoding method that Pechanek disclosed. Pechanek disclosed that the predecoding process generates control signals that are used for execution of the instruction. Predecoding in this type of manner that results in storing some or all of the necessary control signals for the instruction within the actual instruction passed into the processor. The effect of this kind of predecoding means that there is less work for the actual decoder to do when an instruction reaches the decode stage. One of ordinary skill in the art would realize that this can be very beneficial when the decoding stage happens to be in the critical path of the processor, which means that the decoding stage determines how fast the processor can run. If processing from the decoding stage can be moved to a predecoding stage, then the decode stage may no longer be in the critical path of the processor and allows for increased clock speed for instructions executing in the pipeline. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the predecoding method of Pechanek onto the processor of Kotani to allow for increased clock speed on the processor.

Finally, the recent Supreme Court Decision in KSR International Co. v. Teleflex Inc. provides additional rationale for combining the two references together. One of the rationales from the KSR decision allows for combining prior art elements according to known methods to yield predictable results. Combining the well-known method of predecoding instructions to add control signals from Pechanek to the system of Kotani would produce the predictable result of having

instructions that are longer in length than a non-predecoded instruction.

Therefore, the two references can also be correctly combined together in view of KSR International Co. c. Teleflex Inc.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/JAP/

/Jacob A. Petranek/

November 14, 2007

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